TIMING CONTROL MEANS FOR AUTOMATIC COMPENSATION OF TIMING UNCERTAINTIES

Abstract

The present invention relates to the reducing of timing uncertainties in high-performance digital circuitry. More specifically, the present invention relates to a timing control means and method for minimizing timing uncertainties due to skew and jitter. A means for the compensation of timing errors in multiple channel electronic devices comprising at least one register having a plurality of channels comprises: a clock for providing a clock signal; a reference signal generator for generating reference signals for deskewing the registers; wherein for each said register a corresponding feedback loop is associated for the relative alignment of register's timing, the feedback loop comprising a means for detecting a deviation from a predetermined level of probability of reading by said register a desired symbol on a boundary of two reference channel symbols in a sequence and a set of delay means which uses the detected values of probability to generate a feedback signal.

The invention is preferably implemented in a self calibrated receiver and a self calibrating transmitter. Also, the invention can be employed in a digital interface between two items or within a circuit where there is a requirement for tight timing control such as requirement for a low skew between the channels of a register.